PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference UCLARF.003VP	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2004/030580	International filing date *(day/month/year)* 17 September 2004 (17.09.2004)	Priority date *(day/month/year)* 17 September 2003 (17.09.2003)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant THE REGENTS OF THE UNIVERSITY OF CALIFORNIA		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 8 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 21 March 2006 (21.03.2006)
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Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

PCT

To:

see form PCT/ISA/220

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43*bis*.1)

Applicant's or agent's file reference see form PCT/ISA/220	Date of mailing *(day/month/year)* see form PCT/ISA/210 (second sheet) **FOR FURTHER ACTION** See paragraph 2 below
International application No. PCT/US2004/030580	International filing date *(day/month/year)* 17.09.2004
Priority date *(day/month/year)* 17.09.2003	
International Patent Classification (IPC) or both national classification and IPC H03K19/173	
Applicant THE REGENTS OF THE UNIVERSITY OF CALIFORNIA	

1. This opinion contains indications relating to the following items:

- ☑ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2004/030580

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material:

   ☐ in written format

   ☐ in computer readable form

   c. time of filing/furnishing:

   ☐ contained in the international application as filed.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	3,4,10-23,25
	No:	Claims	1,2,5-9,24
Inventive step (IS)	Yes:	Claims	3,4,12,13,21-23
	No:	Claims	1,2,5-11,14-20,24,25
Industrial applicability (IA)	Yes:	Claims	1-25
	No:	Claims	

2. Citations and explanations

see separate sheet

1. The following document is referred to in this communication:

   D(1): TIRI K ET AL: "A Dynamic and Differential CMOS Logic with Signal Independent Power Consumption to Withstand Differential Power Analysis on Smart Cards" ESSCIRC 2002, PROCEEDINGS OF THE 28TH EUROPEAN SOLID-STATE CIRCUIT CONFERENCE, 24-26 SEPT. 2002, FLORENCE, ITALY, 2002, pages 403-406, XP002318805 ISBN: 88-900847-9-0

2. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of independent claims 1 and 24 is not new in the sense of Article 33(2) PCT, whereas the subject-matter of independent claims 10, 19, 20 and 25 does not involve an inventive step within the meaning of Article 33(3) PCT.

2.1 Re claim 1:
Document D(1) discloses an apparatus comprising a sense amplifier based logic gate [D(1), page 405, Figure 4 (left): SABL] having an input network (DPDN), said input network (DPDN) comprising a differential pull-down network (DPDN) [D(1), page 405, Figure 4 (right): transistors receiving inputs A, A\, B, B\], wherein, for a stable input combination, internal nodes of said differential pull-down network are provided to output nodes of said differential pull-down network, cf. page 404, right-hand column, paragraph 2.1. "SABL: basic gate", lines 5-8].

2.2 Re claim 10:
Subject-matter of claim 10 differs from that of claim 1 in that, according to claim 10, a differential pull-up network is employed. It is however already suggested in D(1), page 404, right-hand column, final paragraph, that the SABL gate be also implemented as a "generic p-gate" [with the D(1), Figure 4 circuitry being a "generic n-gate", cf. D(1), page 404, right-hand column, item 2.1., line 5] that precharges to GND and evaluates to VDD through a DPUN, which DPUN obviously is a differential pull-up network.

2.3. Re claim 19:

The Figure 4 circuitry of the D(1) reference is obviously based on a method for transforming a differential pull-down network for a logical function (AND/NAND), comprising:

-- identifying two expressions A and B that combine to the logical function according to a logical AND operation [cf. D(1), Figure 4 (right): left-hand branch], A•B corresponding to a network A and a network B;

-- complementing the expressions in A and B to obtain the dual expression of the logical function, as a logical OR operation A\+B\ [cf. D(1), Figure 4 (right): right-hand branch];

-- transforming the OR operation into a transformed network A\•B+B\, providing the transformed network to an internal node of the A•B network and sharing the network B between the two branches A•B (left-hand side) and A\•B+B\ (right-hand side);

-- repeating the actions of identifying, completing and transforming.

2.4 Re claim 20:
With a two-input AND/NAND operation being equivalent to a NOR/OR operation carried out on inverted input signals, the reasoning set forth under item 2.3 above applies to claim 20 mutatis mutandis.

2.5 Re claim 24:
Document D(1), cf. Figure 6 on page 405, discloses a flip-flop circuit comprising a first sense amplifier logic gate (p-SA) that evaluates on a falling clock edge (cf. page 405, left-hand column, final paragraph, lines 2, 3), said first sense-amplifier logic gate comprising a differential pull-up network (cf. the "generic p-gate" referred to on page 404, right-hand column, final paragraph), said sense amplifier logic gate having a first inverted output and a first non-inverted output (Figure 6: Q\, Q); and said first inverted output and said first non-inverted output provided to a second sense-amplifier logic gate (Figure 6: n-SA) that evaluates on a rising clock edge (cf. page 405, left-hand column, final paragraph, lines 4, 5), said second sense-amplifier logic gate comprising a differential pull-down network (cf. the generic n-gate of Figure 4).

2.6 Re claim 25:
Subject-matter of claim 25 differs from the known circuitry of claim 24 in that, the

order in which the first and second sense-amplifier logic gates are arranged in series is changed. With no particular, unexpected effect resulting therefrom, such modification is not indicative of any inventive step.

3. Dependent claims 2, 4-9, 11, 14-18 (note that "ground" in the ultimate line of claim 14 should correctly read "supply voltage VDD") do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/or inventive step, see document D(1).

4. Claims 21-23:

4.1 Subject-matter of independent claim 21 comprises first and second set-reset latches coupled to each other through an SABL exclusive-or gate. Such circuitry is known in principle from document D(1), cf. Figure 6 and page 405, right-hand column, 1st paragraph. The claim specifies furthermore that the inverted and non-inverted outputs of the second set-reset latch are connected to corresponding inputs of the exclusive-or gate. As can be understood from the present description with regard to the Figure 12 circuitry, the n-xor together with the latches serves as dummy circuitry for an SABL-n-flip-flop (n-SA). The combination of features set forth in claim 21 is neither known from nor rendered obvious by, the available prior art. It appears, however, that the definition of the SABL-n-flip-flop is essential for the performance of the Figure 12 circuitry. An objection under Article 6 PCT for lack of clarity is therefore due to arise.

4.2 Claims 22, 23 are dependent claims within the meaning of Rule 6.4 PCT and are directed to further embodiments of the invention as defined in claim 21.

5. Dependent claims 3, 4, 12, 13 require clarification in the light of description and drawings: The pass-gate introduced in these claims is specified to be "always open" or to be "open" during evaluation. As far as can be understood from the present application documents, the only "dummy pass-gate" disclosed is depicted in present Figure 9, "dummy transistors" (901). This pass-gate is, however, always conducting, i.e. one of the transistors is always closed for providing an electrical connection

between the main terminals of the gate. The above language "pass-gate is closed" is thus interpreted as "pass-gate is open/provides an electrical connection".

On this interpretation, the combination of the features of dependent claims 3, 4, 12, 13 is neither known from, nor rendered obvious by, the available prior art.